Working Group 1
Enabling Technologies

Chair: Sheila Vaidya
Vice Chair: Stu Feldman

WG 1 – Enabling Technologies Charter

- Charter
  - Establish the basic technologies that may provide the foundation for important advances in HEC capability, and determine the critical tasks required before the end of this decade to realize their potential. Such technologies include hardware devices or components and the basic software approaches and components needed to realize advanced HEC capabilities.
- Chair
  - Sheila Vaidya, Lawrence Livermore National Laboratory
- Vice-Chair
  - Stuart Feldman, IBM

WG 1 – Enabling Technologies Guidelines and Questions

- As input to HECRTF charge (1a), Please provide information about key technologies that must be advanced to strengthen the foundation for developing new generations of HEC systems. Include discussion of promising novel hardware and software technologies with potential pay-off for HEC
- Provide brief technology maturity roadmaps and investments, with discussion of costs to develop these technologies
- Discuss technology dependencies and risks (for example, does the roadmap depend on technologies yet to be developed?)
- Example topics:
  - semiconductors, memory (e.g. MRAM), networks (e.g. optical), packaging/cooling, novel logic devices (e.g. RSFQ), alternative computing models

Working Group Participants

- Kamal Abdali, NSF
- Fernand Bedard, NSA
- Herbert Bennett, NIST
- Ivo Bolsens, XILINX
- Jon Boyens, DOC
- Bob Brodersen, UC Berkeley
- Yolanda Comedy, IBM
- Loring Craymer, JPL
- Bronis R. de Supinski, LLNL
- Martin Deneroff, SGI
- Stuart Feldman, IBM *(VICE-CHAIR)*
- Sue Fratkin, CASC
- David Fuller, JNIC/Raytheon
- Gary Hughes, NSA
- Tyce McLarty, LLNL
- Kevin Martin, Georgia Tech
- Virginia Moore, NCO/ITRD
- Ahmed Sameh, Purdue
- John Spargo, Norhrop-Grumman
- William Thigpen, NASA
- Sheila Vaidya, LLNL *(CHAIR)*
- Uzi Vishkin, U Maryland
- Steven Wallach, Chiaro

Timescales

- 0-5 years
  - Suitable for deployment in high-end systems within next 5 years
    - Implies that the technology has been tried and tested in a systems context
    - Requires additional investment beyond commercial industry
- 5-10 years
  - Suitable for deployment in high-end systems in 10 years
    - Implies that the component has been studied and feasibility shown
    - Requires system embodiment and growing investment
- 10+ years
  - New research, not yet reduced to practice
    - Usefulness in systems not yet demonstrated

Interconnects

Passive

- 0-5
  - Optical networking
  - Serial optical interface
- 5-10
  - High-density optical networking
  - Optical packet switching
- 10+
  - Scalability (node density, bandwidth)

Active

- 0-5
  - Electronic cross-bar switch
  - Network processing on board
- 5-10
  - Data Vortex
  - Superconducting cross-bar switch
- 10+

Power/Thermal Management, Packaging

- 0-5
  - Optimization for power efficiency
  - 2.5-D packaging
  - Liquid cooling (e.g., spray)
- 5-10
  - 3-D packaging and cooling (microchannel)
  - Active temperature response
- 10+
  - Higher scalability concepts (improving OPS/W)

Single Chip Architecture

- 0-5
  - Power-efficient designs
  - System on Chip; Processor-in-Memory
  - Reconfigurable circuits
  - Fine-grained irregular parallel computing
- 5-10
  - Adaptive architecture
  - Optical clock distribution
  - Asynchronous designs
- 10+

Memory

Main Memory

- 0-5
  - Optimized memory hierarchy
  - Smart memory controllers
- 5-10
  - 3-D memory (e.g., MRAM)
- 10+
  - Nanoelectronics
  - Molecular electronics

Storage & I/O

- 0-5
  - Object-based storage
  - Remote DMA
  - I/O controllers (MPI, etc.)
- 5-10
  - Software for “cluster” storage access to
  - MRAM, holographic, MEMS, STM, E-beam
- 10+
  - Spectral hole burning
  - Molecular electronics

Device Technologies

- 0-5
  - Silicon on Insulator, SiGe, mixed III-V devices
  - Integrated electro-optic and high-speed electronics
- 5-10
  - Low-temperature CMOS
  - Superconducting - RSFQ
- 10+
  - Nanotechnologies
  - Spintronics

Algorithms, SW-HW Tools

- 0-5
  - Compiler innovations for new architectures
  - Tools for robustness (e.g., delay, fault tolerance)
  - Low-overhead coordination mechanisms
  - Performance monitors
  - Sparse matrix innovations
- 5-10
  - Very High Level Language hardware support
  - Real-time performance monitoring and feedback
  - PRAM (Parallel Random Access Machine model)
- 10+
  - Ideas too numerous to select

Generic Needs

- Sharing
  - NNIN-like consortia
    - National Nanotechnology Infrastructure Network
  - Custom hardware production
  - Intellectual Property policies (open?)
- Tools for
  - Design for Testability
  - Physical design
  - Testing and Verification
  - Simulation
  - Programmability

High-Impact Themes

- 0-5
  - Show value of HEC solutions to the commercial sector
  - Facilitate sharing and collaboration across HEC community
  - Technology
    - Power/thermal management
    - Optical networking
- 5-10
  - Long-term consistent investment in HEC
  - Technology
    - 3-D Packaging
    - New devices (MRAM, MEMS, RSFQ)
    - Power/thermal management & Optical – Ongoing
- 10+ years
  - Continued research for HEC