The International Semiconductor Roadmap and Its Impact on Semiconductor-Related Research

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Gigascale Research Center (GSRC)
The International Technology RoadMap for Semiconductors

- Inaugurated in 1992 (as the NTRS). Initiative of SIA (Semiconductor Industry Association)
- Became an International effort in 1997 (ITRS)
- Provides bi-annual updates on 15 year road-map
- Joint effort of industry, government, consortia, and universities
- An assessment of the semiconductor technology requirements. The objective of the ITRS is to ensure advancements in the performance of integrated circuits.
- Identifies the technological challenges and needs facing the semiconductor industry over the next 15 years.
## A Typical Roadmap Table

### Table 35a High-performance Logic Technology Requirements—Near-term

<table>
<thead>
<tr>
<th></th>
<th>2001</th>
<th>2002</th>
<th>2003</th>
<th>2004</th>
<th>2005</th>
<th>2006</th>
<th>2007</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>YEAR OF PRODUCTION</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DRAM ( \frac{1}{2} ) PITCH (nm)</td>
<td>130</td>
<td>115</td>
<td>100</td>
<td>90</td>
<td>80</td>
<td>70</td>
<td>65</td>
</tr>
<tr>
<td>MPU / ASIC ( \frac{1}{2} ) PITCH (nm)</td>
<td>150</td>
<td>130</td>
<td>107</td>
<td>90</td>
<td>80</td>
<td>70</td>
<td>65</td>
</tr>
<tr>
<td>MPU PRINTED GATE LENGTH (nm)</td>
<td>90</td>
<td>75</td>
<td>65</td>
<td>53</td>
<td>45</td>
<td>40</td>
<td>35</td>
</tr>
<tr>
<td>MPU PHYSICAL GATE LENGTH (nm)</td>
<td>65</td>
<td>53</td>
<td>45</td>
<td>37</td>
<td>32</td>
<td>28</td>
<td>25</td>
</tr>
<tr>
<td>Physical gate length high-performance (HP) (nm) [1]</td>
<td>65</td>
<td>53</td>
<td>45</td>
<td>37</td>
<td>32</td>
<td>28</td>
<td>25</td>
</tr>
<tr>
<td>Equivalent physical oxide thickness for high-performance ( T_{ox} ) (EOT) (nm) [2]</td>
<td>1.3–1.6</td>
<td>1.2–1.5</td>
<td>1.1–1.6</td>
<td>0.9–1.4</td>
<td>0.8–1.3</td>
<td>0.7–1.2</td>
<td>0.6–1.1</td>
</tr>
<tr>
<td>Gate depletion and quantum effects electrical thickness adjustment factor (nm) [3]</td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
<td>0.5</td>
</tr>
<tr>
<td>( T_{ox} ) electrical equivalent (nm) [4]</td>
<td>2.3</td>
<td>2.1</td>
<td>2.0</td>
<td>2.0</td>
<td>1.9</td>
<td>1.9</td>
<td>1.4</td>
</tr>
<tr>
<td>Nominal power supply voltage ( (V_{dd}) ) (V) [5]</td>
<td>1.2</td>
<td>1.1</td>
<td>1.0</td>
<td>1.0</td>
<td>0.9</td>
<td>0.9</td>
<td>0.7</td>
</tr>
<tr>
<td>Nominal high-performance NMOS sub-threshold leakage current, ( I_{leak} ) (at 25 ( ^\circ ) C) (( \mu A ) ( \mu m )) [6]</td>
<td>0.01</td>
<td>0.03</td>
<td>0.07</td>
<td>0.1</td>
<td>0.3</td>
<td>0.7</td>
<td>1</td>
</tr>
<tr>
<td>Nominal high-performance NMOS saturation drive current, ( I_{ds} ) (at ( V_{dd} ) at 25 ( ^\circ ) C) (( \mu A ) ( \mu m )) [7]</td>
<td>900</td>
<td>900</td>
<td>900</td>
<td>900</td>
<td>900</td>
<td>900</td>
<td>900</td>
</tr>
<tr>
<td>Required percent current-drive &quot;mobility/transconductance improvement&quot; [8]</td>
<td>0%</td>
<td>0%</td>
<td>0%</td>
<td>0%</td>
<td>0%</td>
<td>0%</td>
<td>0%</td>
</tr>
<tr>
<td>Parasitic source/drain resistance (Rs) (ohm-( \mu m )) [9]</td>
<td>190</td>
<td>180</td>
<td>180</td>
<td>180</td>
<td>180</td>
<td>170</td>
<td>140</td>
</tr>
<tr>
<td>Parasitic source/drain resistance (Rs) percent of ideal channel resistance ( (V_{dd} I_{dd}) ) [10]</td>
<td>16%</td>
<td>16%</td>
<td>17%</td>
<td>18%</td>
<td>19%</td>
<td>19%</td>
<td>20%</td>
</tr>
<tr>
<td>Parasitic capacitance percent of ideal gate capacitance [11]</td>
<td>19%</td>
<td>22%</td>
<td>24%</td>
<td>27%</td>
<td>29%</td>
<td>32%</td>
<td>27%</td>
</tr>
<tr>
<td>High-performance NMOS device ( \tau (C_{gate} * V_{dd}/ I_{ds}/NMOS)(ps) ) [12]</td>
<td>1.6</td>
<td>1.3</td>
<td>1.1</td>
<td>0.99</td>
<td>0.83</td>
<td>0.76</td>
<td>0.68</td>
</tr>
<tr>
<td>Relative device performance [13]</td>
<td>1.0</td>
<td>1.2</td>
<td>1.5</td>
<td>1.6</td>
<td>2.0</td>
<td>2.1</td>
<td>2.5</td>
</tr>
<tr>
<td>Energy per ( (W/L_{gate}) ) device switching transition ( (C_{gate} (3 L_{gate}) V^{2}) ) ( (f/H) Device) [14]</td>
<td>0.347</td>
<td>0.212</td>
<td>0.137</td>
<td>0.099</td>
<td>0.065</td>
<td>0.052</td>
<td>0.032</td>
</tr>
<tr>
<td>Static power dissipation per ( (W/L_{gate}) ) device (Watts/Device) [15]</td>
<td>5.6E-09</td>
<td>6.7E-09</td>
<td>1.0E-08</td>
<td>1.1E-08</td>
<td>2.6E-08</td>
<td>5.3E-08</td>
<td>5.3E-08</td>
</tr>
</tbody>
</table>
### Table 35b High-performance Logic Technology Requirements—Long-term

<table>
<thead>
<tr>
<th>YEAR OF PRODUCTION</th>
<th>2010</th>
<th>2013</th>
<th>2016</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRAM ½ Pitch (nm)</td>
<td>45</td>
<td>32</td>
<td>22</td>
</tr>
<tr>
<td>MPU / ASIC ½ Pitch (nm)</td>
<td>50</td>
<td>35</td>
<td>25</td>
</tr>
<tr>
<td>MPU Printed Gate Length (nm)</td>
<td>25</td>
<td>18</td>
<td>13</td>
</tr>
<tr>
<td>MPU Physical Gate Length (nm)</td>
<td>18</td>
<td>13</td>
<td>9</td>
</tr>
<tr>
<td>Physical gate length high-performance (HP) (nm) [1]</td>
<td>18</td>
<td>13</td>
<td>9</td>
</tr>
<tr>
<td>Equivalent physical oxide thickness for high-performance T&lt;sub&gt;ox&lt;/sub&gt; (EOT) (nm) [2]</td>
<td>0.5-0.8</td>
<td>0.4-0.6</td>
<td>0.4-0.5</td>
</tr>
<tr>
<td>Gate depletion and quantum effects electrical thickness adjustment factor (nm) [3]</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>T&lt;sub&gt;ox&lt;/sub&gt; electrical equivalent (nm) [4]</td>
<td>1.2</td>
<td>1.0</td>
<td>0.9</td>
</tr>
<tr>
<td>Nominal power supply voltage (V&lt;sub&gt;dd&lt;/sub&gt;) (V) [5]</td>
<td>0.6</td>
<td>0.5</td>
<td>0.4</td>
</tr>
<tr>
<td>Nominal high-performance NMOS sub threshold leakage current, I&lt;sub&gt;d,leak&lt;/sub&gt; (at 25°C) (μA/μm) [6]</td>
<td>3</td>
<td>7</td>
<td>10</td>
</tr>
<tr>
<td>Nominal high-performance NMOS saturation drive current, I&lt;sub&gt;d,sat&lt;/sub&gt; (at V&lt;sub&gt;dd&lt;/sub&gt;, at 25°C) (μA/μm) [7]</td>
<td>1200</td>
<td>1500</td>
<td>1500</td>
</tr>
<tr>
<td>Required percent current-drive &quot;mobility/transconductance improvement&quot; [8]</td>
<td>30%</td>
<td>70%</td>
<td>100%</td>
</tr>
<tr>
<td>Parasitic source/drain resistance (R&lt;sub&gt;sd&lt;/sub&gt;) (ohm-μm) [9]</td>
<td>110</td>
<td>90</td>
<td>80</td>
</tr>
<tr>
<td>Parasitic source/drain resistance (R&lt;sub&gt;sd&lt;/sub&gt;) percent of ideal channel resistance (V&lt;sub&gt;dd&lt;/sub&gt;/I&lt;sub&gt;dd&lt;/sub&gt;) [10]</td>
<td>25%</td>
<td>30%</td>
<td>35%</td>
</tr>
<tr>
<td>Parasitic capacitance percent of ideal gate capacitance [11]</td>
<td>31%</td>
<td>36%</td>
<td>42%</td>
</tr>
<tr>
<td>High-performance NMOS device t (C&lt;sub&gt;gate&lt;/sub&gt; * V&lt;sub&gt;dd&lt;/sub&gt; / I&lt;sub&gt;dd&lt;/sub&gt;-NMOS)(ps) [12]</td>
<td>0.39</td>
<td>0.22</td>
<td>0.15</td>
</tr>
<tr>
<td>Relative device performance [13]</td>
<td>4.3</td>
<td>7.2</td>
<td>10.7</td>
</tr>
<tr>
<td>Energy per (W/L&lt;sub&gt;gate&lt;/sub&gt;=3) device switching transition (C&lt;sub&gt;gate&lt;/sub&gt;<em>(3</em>I&lt;sub&gt;gate&lt;/sub&gt;)*V&lt;sup&gt;2&lt;/sup&gt;) (μJ/Device) [14]</td>
<td>0.015</td>
<td>0.007</td>
<td>0.002</td>
</tr>
<tr>
<td>Static power dissipation per (W/Lgate=3) device (Watts/Device) [15]</td>
<td>9.7E-08</td>
<td>1.4E-07</td>
<td>1.1E-07</td>
</tr>
</tbody>
</table>

*White—Manufacturable Solutions Exist, and Are Being Optimized
Yellow—Manufacturable Solutions are Known
Red—Manufacturable Solutions are NOT Known
More Sophistication over the Years

The “Living” ITRS Roadmap (started in 2001)

◆ Provides: consistency checks, unified assumptions for power, frequency, die size, density, performance, etc

◆ Creates linkages between different areas

◆ Improves flexibility, quality, transparency of roadmapping

→ Quantified Power Management Gap (High-Performance MPU) for Design Technology
### Important Outcome: Challenges and Roadblocks

#### DESIGN

<table>
<thead>
<tr>
<th>Difficult Challenges</th>
<th>Summary of Issues</th>
</tr>
</thead>
<tbody>
<tr>
<td>Productivity</td>
<td>To avoid exponentially increasing design cost, overall productivity of designed functions on chip must scale at &gt; 2x per node. Reuse productivity (including migration) of design, verification and test must also scale at &gt; 2x per node.</td>
</tr>
<tr>
<td>Power</td>
<td>Non-ideal scaling of planar CMOS devices, together with the roadmap for interconnect materials and package technologies, presents a variety of challenges related to power management and current delivery.</td>
</tr>
<tr>
<td>Manufacturing Integration</td>
<td>“Red bricks”—technology requirements for which no known solutions exist—are increasingly common throughout the ITRS. On the other hand, challenges that are impossible to solve within a single technology area of the ITRS may be solvable (more cost-effectively) with appropriate intervention from, or partnership with, DT. Feasibility of future technology nodes will come to depend on such “sharing of red bricks.”</td>
</tr>
<tr>
<td>Interference</td>
<td>Resource-efficient communication and synchronization, already challenged by global interconnect scaling trends, are increasingly hampered by noise and interference. Prevailing signal integrity methodologies in logical, circuit and physical design, while apparently scalable through the 100 nm node, are reaching their limits of practicality.</td>
</tr>
<tr>
<td>Error Tolerance</td>
<td>Relaxing the requirement of 100% correctness for devices and interconnects may dramatically reduce costs of manufacturing, verification, and test. Such a paradigm shift is likely forced in any case by technology scaling, which leads to more transient and permanent failures of signals, logic values, devices, and interconnects.</td>
</tr>
</tbody>
</table>
Example: The Productivity Gap

Source: SEMATECH
Focus Center Research Program

Origin of This Program

- Bill Perry
- Paul Kaminski
- Anita Jones
- Dan Radack
- Gordon Moore
- Craig Barrett
- Larry Sumney
- Harold Hosack

U.S. Universities--Our National Treasure

Semiconductor Technology Council Co-Chairs

OSD/MARCO Agreement

DARPA/MARCO Joint Solicitation & Management
The objective of the FCRP is the establishment of focused multi-university teams to engage in discovery research in areas where evolutionary research and development have failed to find solutions to anticipated problems for the semiconductor industry.
DoD Motivation:
DoDs Biggest Error in Dealing With ICs:

Thinking They Could Just Buy Commercial Parts

DoD/Industry/University Partnerships

Focus Centers

Design
Interconnect
Mat & Struc./Devices
Ckts/Sys/Software

Industry
Solves ITRS
Roadblocks

Programs of Opportunity

PCA (ITO-Graybill)
ASIC (MTO-Reuss)
TEAM (MTO-Reuss)
Hyperscale (MTO)
Noise Radar (MTO)

DoD/Industry/University Partnerships

US and Japanese Semiconductor Market Share

source: SIA Projections, VLSI Research Actuals

15%
65%

Japan projected
45.3%
40.8
(actual)

US projected
40.8
(actual)

SEMATECH

DoD Use of ICs Fall Behind Commercial Market

DoD Hands Off Policy

VHSIC

1.25µ

0.5µ


Minuteman II
Production
Orders Ignite
IC Industry

DoD R&D
Leads to IC Invention


DoD Ignoites Chipmakers

87 to 97

67 to 87

47 to 67
Focus Center Research Program

Design and Test Focus Center
Mission: To empower designers to move from ad-hoc SOC design to disciplined, platform-based design by enabling scalable, heterogeneous, component-based design with a single-pass route to efficient Si implementation from a microarchitecture.

Interconnect Focus Center
The IFC is a comprehensive effort to provide a hierarchy of interconnect solutions with an optimum interconnect possessing low latency and little energy dissipation through:
• innovative system architectures
• original circuit concepts
• novel interconnect structures
• new materials and processes
• previously untapped fundamental principles

Materials Structures & Devices Focus Center
The MSD Center is focused on exploring the most promising path for microelectronic device evolution in the next 2-3 decades. There are 2 overlapping approaches:
• Scaling CMOS to its ultimate limit
  • gate length L < 15 nm
  • operating voltage < 0.5v
  • novel mats & structures added to Si
• Exploration of new frontier devices
  • high speed/low power transistor alternatives

Circuits, Systems & Software Focus Center
The C2S2 mission is twofold:
• Develop the fundamental new methods needed to convert tomorrow's transistors into useful performance.
• Mitigate impacts and exploit opportunities in design of circuits, systems and software.
• In other words, how fast, how small, how cheap and how quickly can they be designed??

Research Teams:

UC-Berkeley
CMU    UCLA
MIT    UC – San Diego
Penn State    UC – Santa Barbara
Princeton    UC – Santa Cruz
Purdue    Univ. of Michigan
Stanford    UT Austin
Univ. of Wisconsin

Georgia Tech
MIT
Stanford
RPI
UCLA
Univ. of Albany

MIT
Cornell    UC-Berkeley
Princeton    Univ. of Albany
Purdue    UT-Austin
Stanford    UVA
UCLA

CMU
Columbia    RPI
Cornell    Stanford
MIT    UC–Berkeley
Princeton    UIUC
Univ. of Washington

Sponsors:

Agere    Intel
Agilent    LSI Logic
AMD    Micron
Analog Devices    Motorola
Conexant    National
Cypress    TI
IBM    Xilinx

Semiconductor Industry Suppliers

Air Products    SCP Global
Applied Materials    Speedfam
KLA-Tencor    Teradyne
Novellus    Veriflo

DUSD(S&T)

Deputy Undersecretary of Defense for Science & Technology

DARPA

Prof. Jan Rabaey

Prof. James Meindl

Prof. Dimitri Antoniadis

Prof. Rob Rutenbar
## Focus Center Research Program Funding

<table>
<thead>
<tr>
<th>Source</th>
<th>1999 (FY98)</th>
<th>2000 (99/00)</th>
<th>2001 (FY01)</th>
<th>2002 (FY02)</th>
<th>2003 (FY03)</th>
<th>2004 (FY04)</th>
<th>2005 (FY05)</th>
<th>2006 (FY06)</th>
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</thead>
<tbody>
<tr>
<td>SIA Members</td>
<td>4</td>
<td>6</td>
<td>11</td>
<td>12</td>
<td>20</td>
<td>26</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>Suppliers + Fabless</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>4</td>
<td>10</td>
<td>13</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>DUSD(LABS)</td>
<td>4</td>
<td>7</td>
<td>3</td>
<td>8</td>
<td>10</td>
<td>13</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td><strong>TOTAL FCRP</strong></td>
<td><strong>$10</strong></td>
<td><strong>$16</strong></td>
<td><strong>$18</strong></td>
<td><strong>$24</strong></td>
<td><strong>$40</strong></td>
<td><strong>$52</strong></td>
<td><strong>$60</strong></td>
<td><strong>$60</strong></td>
</tr>
</tbody>
</table>

### Focus Centers Funding Schedule ($M)

| Focus Center #5 | 3          | 6          | 10         | 10         | 10         |
| Focus Center #6 | 3          | 6          | 10         | 10         | 10         |

**TOTAL FC** | **$11** | **$12** | **$22** | **$24** | **$40** | **$52** | **$60** | **$60** |

## DARPA Demonstration Funding

| DARPA DEMO #1 | 1 | 6 | 10 | 9 | 4 |
| DARPA DEMO #2 | 1 | 6 | 10 | 9 |
| DARPA DEMO #3 | 1 | 6 | 10 |
| DARPA DEMO #4 | 1 | 6 |
| DARPA DEMO #5 | 1 |

**TOTAL DARPA** | **28** | **$1** | **$7** | **$17** | **$26** | **$30** |
**GSRC (and FCRP)?**

**“Not Just Research As Usual”**

- A unique experiment in long-range, collaborative research, enabling broad collaboration across many areas of EDA and Design.

- In the 1960-1980’s DARPA played a key role in creating and maintaining a collaborative community in design and architecture:
  - Xerox PARC & the Alto, Berkeley Unix, RISC, RAID, Integrated EDA Systems…

- GSRC is about rebuilding and maintaining such a community of researchers in many fields related to silicon design productivity.
Summary

◆ The ITRS Roadmap had done a superb job in keeping the semiconductor industry focused and forward-looking.
◆ It has helped to identify major roadblocks, and has sensitized the industry and government to invest in long-term research. The Marco FCRP is a perfect example of this.
◆ Beware of the pitfalls of road-mapping. As a mostly extrapolative exercise, it fails to capture technology surprises.