The International Semiconductor Roadmap and Its Impact on Semiconductor-Related Research

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The International Technology RoadMap for Semiconductors

- Inaugurated in 1992 (as the NTRS). Initiative of SIA (Semiconductor Industry Association)
- Became an International effort in 1997 (ITRS)
- Provides bi-annual updates on 15 year road-map
- Joint effort of industry, government, consortia, and universities
- An assessment of the semiconductor technology requirements. The objective of the ITRS s to ensure advancements in the performance of integrated circuits.
- Identifies the technological challenges and needs facing the semiconductor industry over the next 15 years.

A Typical Roadmap Table

Table 35a High-performance Logic Technology Requirements—Near-term

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM ½ PITCH (nm)	130	115	100	90	80	70	65
MPU / ASIC ½ PITCH (nm)	150	130	107	90	80	70	65
MPU PRINTED GATE LENGTH (nm)	90	75	65	53	45	40	35
MPU PHYSICAL GATE LENGTH (nm)	65	53	45	37	32	28	25
Physical gate length high-performance (HP) (nm) [1]	65	53	45	37	32	28	25
Equivalent physical oxide thickness for high-performance T_{ox} (EOT)(nm) [2]	1.3–1.6	1.2–1.5	1.1–1.6	0.9–1.4	0.8–1.3	0.7–1.2	0.6–1.1
Gate depletion and quantum effects electrical thickness adjustment factor (nm) [3]	0.8	0.8	0.8	0.8	0.8	0.8	0.5
T_{ox} electrical equivalent (nm) [4]	2.3	2.1	2.0	2.0	1.9	1.9	1.4
Nominal power supply voltage (V_{dd}) (V) [5]	1.2	1.1	1.0	1.0	0.9	0.9	0.7
Nominal high-performance NMOS sub-threshold leakage current, $I_{sd,leak}$ (at 25 °C) (μA/μm) [6]	0.01	0.03	0.07	0.1	0.3	0.7	1
Nominal high-performance NMOS saturation drive current, I_{dd} (at V_{dd}, at 25 °C) (μA/μm) [7]	900	900	900	900	900	900	900
Required percent current-drive "mobility/transconductance improvement" [8]	0%	0%	0%	0%	0%	0%	0%
Parasitic source/drain resistance (Rsd) (ohm-μm) [9]	190	180	180	180	180	170	140
Parasitic source/drain resistance (Rsd) percent of ideal channel resistance (V_{dd}/I_{dd}) [10]	16%	16%	17%	18%	19%	19%	20%
Parasitic capacitance percent of ideal gate capacitance [11]	19%	22%	24%	27%	29%	32%	27%
High-performance NMOS device τ (C_{gate} * V_{dd} / I_{dd}-NMOS)(ps) [12]	1.6	1.3	1.1	0.99	0.83	0.76	0.68
Relative device performance [13]	1.0	1.2	1.5	1.6	2.0	2.1	2.5
Energy per (W/L_{gate}=3) device switching transition (C_{gate}*(3*L_{gate})*V^2) (fJ/Device) [14]	0.347	0.212	0.137	0.099	0.065	0.052	0.032
Static power dissipation per (W/Lgate=3) device (Watts/Device) [15]	5.6E-09	6.7E-09	1.0E-08	1.1E-08	2.6E-08	5.3E-08	5.3E-08

A Typical Roadmap Table (cntd)

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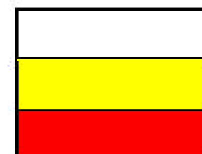
Table 35b High-performance Logic Technology Requirements—Long-term

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ PITCH (nm)	45	32	22
MPU / ASIC ½ PITCH (nm)	50	35	25
MPU PRINTED GATE LENGTH (nm)	25	18	13
MPU PHYSICAL GATE LENGTH (nm)	18	13	9
Physical gate length high-performance (HP) (nm) [1]	18	13	9
Equivalent physical oxide thickness for high-performance T_{ox} (EOT)(nm) [2]	0.5-0.8	0.4-0.6	0.4-0.5
Gate depletion and quantum effects electrical thickness adjustment factor (nm) [3]	0.5	0.5	0.5
T_{ox} electrical equivalent (nm) [4]	1.2	1.0	0.9
Nominal power supply voltage (V_{dd}) (V) [5]	0.6	0.5	0.4
Nominal high-performance NMOS sub threshold leakage current, $I_{sd,leak}$ (at 25°C) (µA/µm) [6]	3	7	10
Nominal high-performance NMOS saturation drive current , I_{dd} (at V_{dd}, at 25°C) (µA/µm) [7]	1200	1500	1500
Required percent current-drive "mobility/transconductance improvement" [8]	30%	70%	100%
Parasitic source/drain resistance (Rsd) (ohm-µm) [9]	110	90	80
Parasitic source/drain resistance (Rsd) percent of ideal channel resistance (V_{dd}/I_{dd}) [10]	25%	30%	35%
Parasitic capacitance percent of ideal gate capacitance [11]	31%	36%	42%
High-performance NMOS device τ (C_{gate} * V_{dd} / I_{dd}-NMOS)(ps) [12]	0.39	0.22	0.15
Relative device performance [13]	4.3	7.2	10.7
Energy per (W/L_{gate}=3) device switching transition (C_{gate}*(3*L_{gate})*V^2) (fJ/Device) [14]	0.015	0.007	0.002
Static power dissipation per (W/Lgate=3) device (Watts/Device) [15]	9.7E-08	1.4E-07	1.1E-07

White—Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red—Manufacturable Solutions are NOT Known



More Sophistication over the Years

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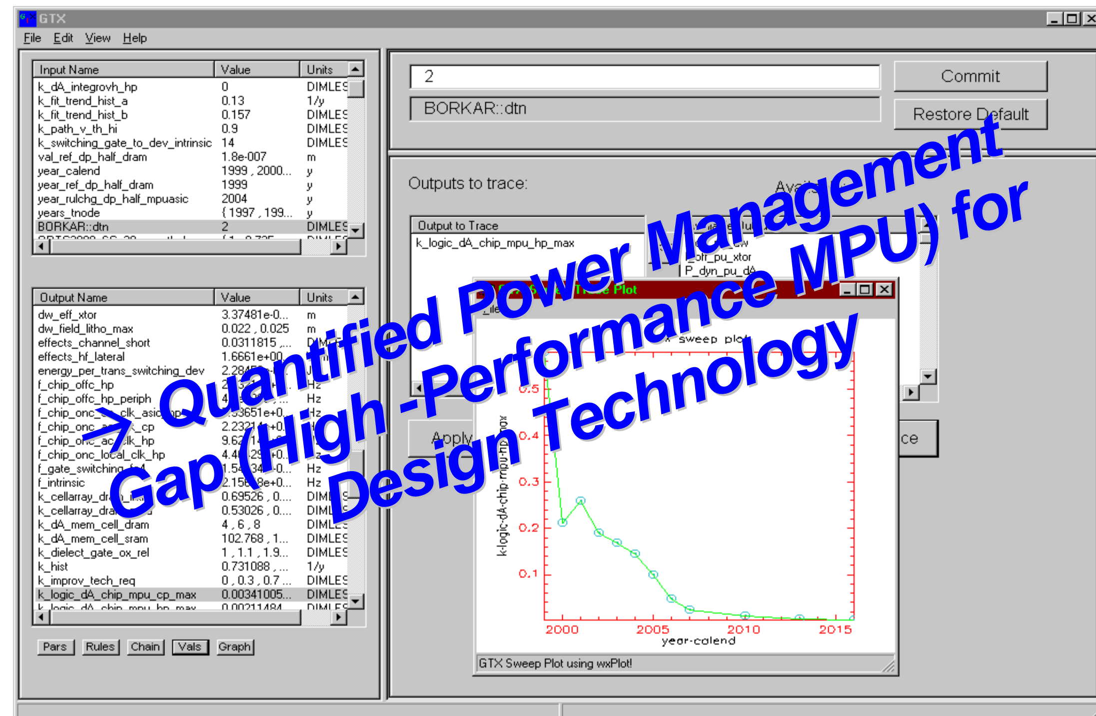
The “Living” ITRS Roadmap (started in 2001)

◆ Provides: consistency checks, unified assumptions for power, frequency, die size, density, performance, etc

◆ Creates linkages between different areas

◆ Improves flexibility, quality, transparency of roadmapping

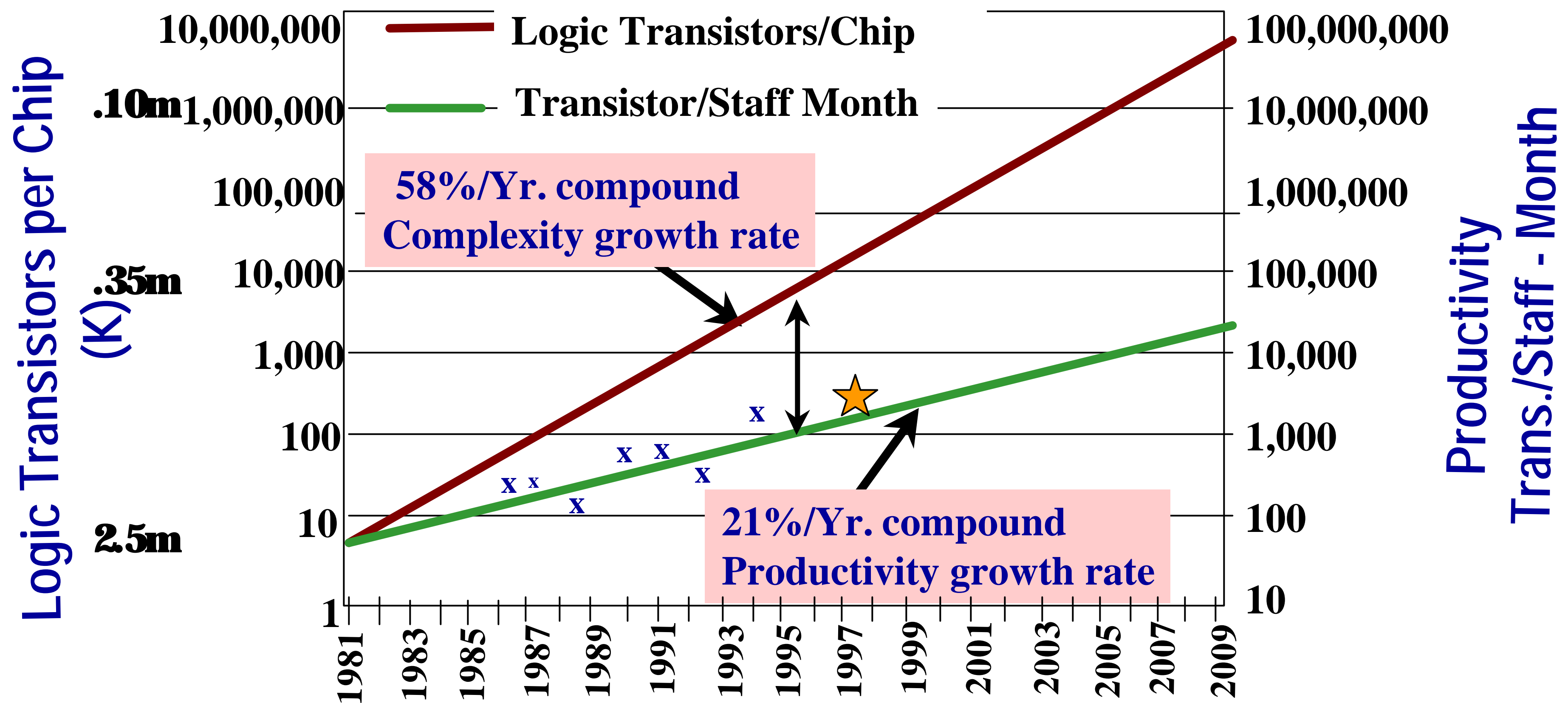


Important Outcome: Challenges and Roadblocks

DESIGN

Difficult Challenges	*Summary of Issues*
Productivity	To avoid exponentially increasing design cost, overall productivity of designed functions on chip must scale at > 2× per node. Reuse productivity (including migration) of design, verification and test must also scale at > 2× per node.
Power	Non-ideal scaling of planar CMOS devices, together with the roadmap for interconnect materials and package technologies, presents a variety of challenges related to power management and current delivery.
Manufacturing Integration	"Red bricks"—technology requirements for which no known solutions exist—are increasingly common throughout the *ITRS*. On the other hand, challenges that are impossible to solve within a single technology area of the *ITRS* may be solvable (more cost-effectively) with appropriate intervention from, or partnership with, DT. Feasibility of future technology nodes will come to depend on such "sharing of red bricks."
Interference	Resource-efficient communication and synchronization, already challenged by global interconnect scaling trends, are increasingly hampered by noise and interference. Prevailing signal integrity methodologies in logical, circuit and physical design, while apparently scalable through the 100 nm node, are reaching their limits of practicality.
Error Tolerance	Relaxing the requirement of 100% correctness for devices and interconnects may dramatically reduce costs of manufacturing, verification, and test. Such a paradigm shift is likely forced in any case by technology scaling, which leads to more transient and permanent failures of signals, logic values, devices, and interconnects.

Example: The Productivity Gap



Source: SEMATECH

Focus Center Research Program

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Origin of This Program

- Bill Perry
- Gordon Moore

U.S. Universities--Our National Treasure

- Paul Kaminski
- Craig Barrett

Semiconductor Technology Council Co-Chairs

- Anita Jones
- Larry Sumney

OSD/MARCO Agreement

- Dan Radack
- Harold Hosack

DARPA/MARCO Joint Solicitation & Management

Industry Motivation

Critical problems accelerate toward us--In 2 years time, the red areas are 3 years closer!

1997 NTRS Tables

2006
100nm

Table 14 Memory and Logic Technology Requiremen

Year of First Product Shipment Technology Generation	1997 250 nm	1999 180 nm	2001 150 nm	2003 130 nm	2006 100 nm	2009 70 nm	2012 50 nm
Min. Logic Vdd (V) (desktop)	2.5–1.8	1.8–1.5	1.5–1.2	1.5–1.2	1.2–0.9	0.9–0.6	0.6–0.5
V_{dd} Variation	£ 10%	£ 10%	£10%	£10%	£10%	£ 10%	£ 10%
T_{ox} Equivalent (nm)	4–5	3–4	2–3	2–3	1.5–2	< 1.5	< 1.0
Equivalent Maximum E-field (MV/cm)	4–5	5	5	5	> 5	> 5	> 5
Max I_{off} @ 25°C (nA/μm) (For minimum L device)	1	1	3	3	3	10	10
Nominal I_{on} @ 25°C (μA/μm) (NMOS/PMOS)	600/280	600/280	600/280	600/280	600/280	600/280	600/280
Gate Delay Metric (CV/I) (ps)*	16–17	12–13	10–12	9–10	7	4–5	3–4
V_T 3s Variation (± mV) (For minimum L device)	60	50	45	40	40	40	40
L_{gate} 3s Variation (For nominal device)	£ 10%	£ 10%	£10%	£10%	£10%	£ 10%	£ 10%
L_{eff} 3s Variation (For nominal device; % of L_{eff})	£ 20%	£ 20%	£20%	£20%	£20%	£ 20%	£ 20%
S/D Extension Junction Depth, Nominal (nm)	50–100	36–72	30–60	26–52	20–40	15–30	10–20
Total Series Resistance of S/D (% of channel resistance)	£ 10%	£ 10%	£10%	£10%	£10%	£ 10%	£ 10%
Gate Sheet Resistance (W/sq)	4–6	4–6	4–6	4–6	4–6	< 5	< 5
Isolation Pitch	Consistent with the linear scaling per generation						
Interconnect Levels	6	6–7	7	7	7–8	8–9	9
Short Wire Pitch (μm)	0.50–0.75	0.36–0.54	0.30–0.45	0.26–0.39	0.2–0.3	0.14–0.21	0.10–0.15
DRAM Cell Size ($μm^2$)	0.56	0.22	0.14	0.09	0.036	0.014	0.006
Soft Error Rate (FITs)	1000	1000	1000	1000	1000	1000	1000
DRAM Retention Time (ms)	64–128	128–256	–	256–512	512–1024	1024–2048	2048–4096
Flash Data Retention (year)	10	10	10	10	10	10	10
NOR Cell Size ($μm^2$)	0.6	0.3	0.22	0.15	0.08	0.04	0.02
+/– Vpp	8.5	8	8	7.5	7	6.5	6
Tunnel Oxide (nm)	8.5	8	8	7.5	7	6.5	6

1999 ITRS Tables

2005
100nm

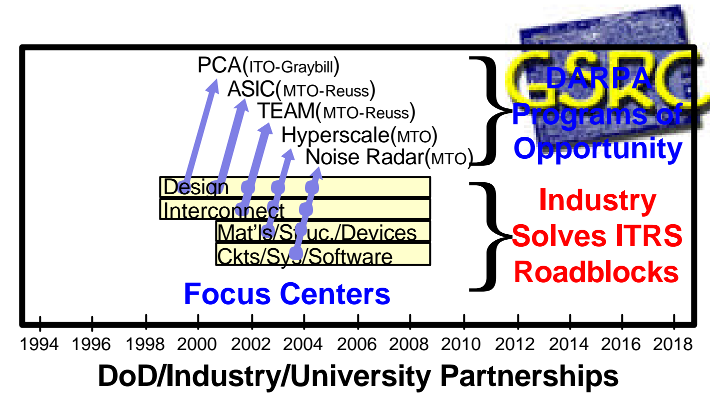
TWG Technology Requirements

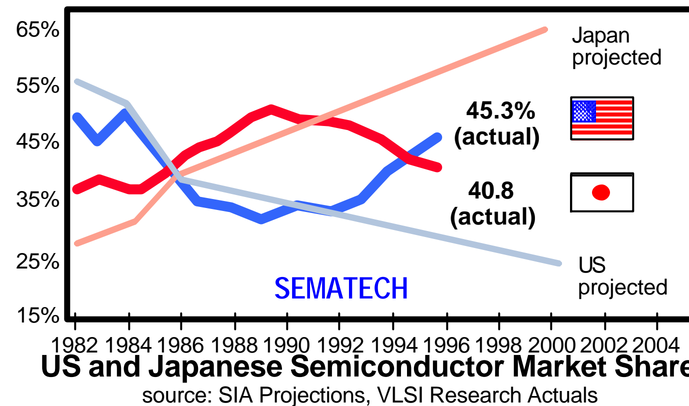
	1999 180	2002 130 nm	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
Min. Logic V_{dd} (V) (desktop)	1.8 - 1.5	1.5 - 1.2	1.2 - 0.9	0.9 - 0.6	0.6 - 0.5	0.6 - 0.3*
Tox equivalent (nm)	2.-3	1.5-2	<1.5	<1	< 1.0	< 1.0
Max I_{off} @ 25 °C (nA/μm) (For min. L device) High Perf.	5	5	4	3	3	2
Nominal I_{on} @ 25 °C (μA/μm) [NMOS/PMOS] High Perf.	750/350	750/350	750/350	750/350	750/350	750/350
Max I_{off} @ 25 °C (pA/μm) (For min. L device) Low Power	4.71E+02	10	10	10	10	10
Nominal I_{on} @ 25 °C (μA/μm) [NMOS/PMOS] Low Power	450/210	450/210	450/210	450/210	450/210	450/210
V_T 3σ variation (±mV) (For min. L device)	50	42	33	25	17	17
S/D extension junction depth, nominal (μm)	0.045 - 0.07	0.03 - 0.05	0.025 - 0.0	0.02 - 0.028	0.013 - 0.02	0.01 - 0.014
Gate sheet resistance (Ω/sq) @ minimum dimension	4 - 6	4 - 6	4 - 6	<5	<5	<5
Interconnect Levels	6--7	7	7--8	8	8-9	9
Short wire pitch (μm)	0.36 - 0.54	0.26 - 0.39	0.2 - 0.3	0.14 - 0.21	0.10 - 0.15	0.07 - 0.11
DRAM cell size ($μm^2$)	0.26 - 0.32	0.13 - 0.17	0.06 - 0.08	0.03 - 0.04	0.015 - 0.02	0.0074 - 0.0098
Cell Dielectric Tox Equivalent (nm)	3.3 - 4.3	1.7 - 2.7	1.15	0.7 - 1.0	0.5	0.4
Min. Refresh Time (ms)	250	220	220	200	200	200

The objective of the FCRP is the establishment of focused multi-university teams to engage in discovery research in areas where evolutionary research and development have failed to find solutions to anticipated problems for the semiconductor industry.

DoD Motivation:
DoDs Biggest Error in Dealing With ICs:

Thinking They Could Just Buy Commercial Parts





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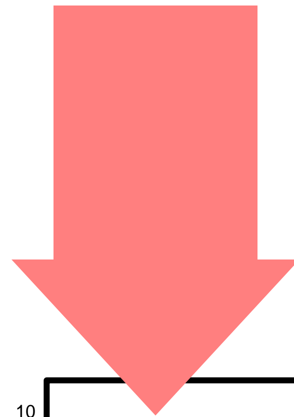

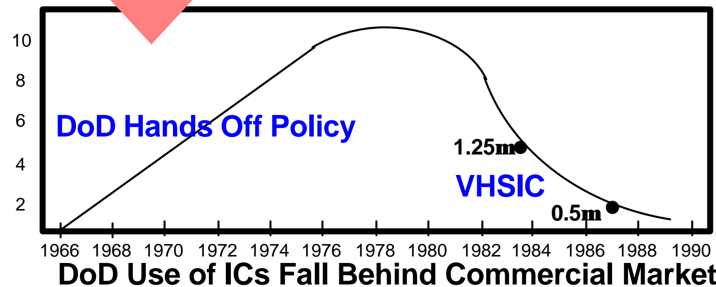

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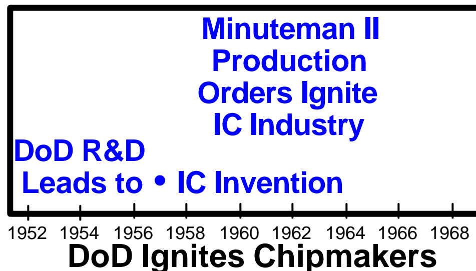

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Focus Center Research Program Structure

Funding Sources	Semiconductor Industry Suppliers	SIA	DoD	Other Potential Sources

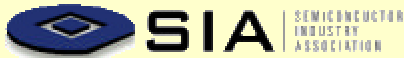
Focus Center Management: MARCO/DARPA ← Governing Council

Lead Universities: Design/Test, Interconnect, Materials, Structures, Devices, Circuits, Systems, Software, #5, #6

Affiliated Universities

Focus Center Research Program

Sponsors:



Agere	Intel
Agilent	LSI Logic
AMD	Micron
Analog Devices	Motorola
Conexant	National
Cypress	TI
IBM	Xilinx

Semiconductor Industry Suppliers

Air Products	SCP Global
Applied Materials	Speedfam
KLA-Tencor	Teradyne
Novellus	Veriflo

DUSD(S&T)

Deputy Undersecretary of Defense for Science & Technology

Design and Test Focus Center

Prof. Jan Rabaey

Mission: To empower designers to move from ad-hoc SOC design to disciplined, **platform-based design** by enabling scalable, heterogeneous, component-based design with a single-pass route to efficient Si implementation from a microarchitecture.

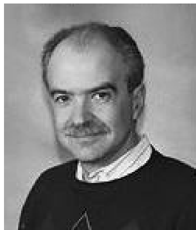
Interconnect Focus Center

Prof. James Meindl

The IFC is a comprehensive effort to provide a hierarchy of interconnect solutions with an optimum interconnect possessing low latency and little energy dissipation through:

- innovative system architectures
- original circuit concepts
- novel interconnect structures
- new materials and processes
- previously untapped fundamental principles

Materials Structures & Devices Focus Center



Prof. Dimitri Antoniadis

The MSD Center is focused on exploring the most promising path for microelectronic device evolution in the next 2-3 decades. There are 2 overlapping approaches:

- Scaling CMOS to its ultimate limit
    - gate length L< 15 nm
    - operating voltage < 0.5v
    - novel matls & structures added to Si
- Exploration of new frontier devices
    - high speed/low power transistor alternatives

Circuits, Systems & Software Focus Center

Prof. Rob Rutenbar

The C2S2 mission is twofold:

- Develop the fundamental new methods needed to convert tomorrow's transistors into useful performance.
- Mitigate impacts and exploit opportunities in design of circuits, systems and software.
- In other words, how fast, how small, how cheap and how quickly can they be designed??

Research Teams:

UC-Berkeley

CMU	UCLA
MIT	UC – San Diego
Penn State	UC – Santa Barbara
Princeton	UC – Santa Cruz
Purdue	Univ. of Michigan
Stanford	UT Austin
Univ. of Wisconsin	

Georgia Tech

MIT
Stanford
RPI
UCLA
Univ. of Albany

MIT

Cornell	UC-Berkeley
Princeton	Univ. of Albany
Purdue	UT-Austin
Stanford	UVA
UCLA	

CMU

Columbia	RPI
Cornell	Stanford
MIT	UC–Berkeley
Princeton	UIUC
Univ. of Washington	

Focus Center Research Program Funding

Source	1999 (FY98)	2000 (99/00)	2001 (FY01)	2002 (FY02)	2003 (FY03)	2004 (FY04)	2005 (FY05)	2006 (FY06)
SIA Members	4	6	11	12	20	26	30	30
Suppliers + Fabless	2	3	4	4	10	13	15	15
DUSD(LABS)	4	7	3	8	10	13	15	15
TOTAL FCRP	$10	$16	$18	$24	$40	$52	$60	$60
Focus Centers			**Funding Schedule ($M)**					
UCB - Design & Test	5	6	9	9	10	10	10	10
GIT - Interconnect	6	6	7	7	10	10	10	10
MIT - Mtls, Structures & Devices			3	4	7	10	10	10
CMU - Ckts, Sys. & Software			3	4	7	10	10	10
Focus Center # 5					3	6	10	10
Focus Center # 6					3	6	10	10
TOTAL FC	$11	$12	$22	$24	$40	$52	$60	$60

DARPA Demonstration Funding

	1999 (FY98)	2000 (99/00)	2001 (FY01)	2002 (FY02)	2003 (FY03)	2004 (FY04)	2005 (FY05)	2006 (FY06)
DARPA DEMO #1				1	6	10	9	4
DARPA DEMO #2					1	6	10	9
DARPA DEMO #3						1	6	10
DARPA DEMO #4							1	6
DARPA DEMO #5								1
TOTAL DARPA				$1	$7	$17	$26	$30

GSRC (and FCRP)? “Not Just Research As Usual”

- A unique experiment in long-range, collaborative research, enabling broad collaboration across many areas of EDA and Design
- In the 1960-1980’s DARPA played a key role in creating and maintaining a collaborative community in design and architecture
  - Xerox PARC & the Alto, Berkeley Unix, RISC, RAID, Integrated EDA Systems…
- GSRC is about rebuilding and maintaining such a community of researchers in many fields related to silicon design productivity

Summary

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- The ITRS Roadmap had done a superb job in keeping the semiconductor industry focused and forward-looking.
- It has helped to identify major roadblocks, and has sensitized the industry and government to invest in long-term research. The Marco FCRP is a perfect example of this.
- Beware of the pitfalls of road-mapping. As a mostly extrapolative exercise, it fails to capture technology surprises.