

## **CRA Conference on “Grand Research Challenges” in Computer Science and Engineering**

### **Enabling Nanotechnology for Ubiquitous Computers**

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The prediction is that Moore’s Law will be alive and well for at least the next decade. However, CMOS technology roadblocks to be faced include fundamental power limitations, overall design complexity limits due to increasing design effort/costs, dramatic increases in fabrication costs (especially mask costs), scaling issues limiting global interconnect wiring performance, increasing error rates with decreasing feature sizes, and chip I/O bottlenecks (increasing Rent’s exponent). To quote Patrick Gelsinger (Vice President and Chief Technology Officer at Intel) in a recent article in *CACM*, “The economic and physics challenges of maintaining Moore’s Law continue to exist . . . <but> do not fundamentally deter Moore’s Law for at least the next decade.” He goes on to say that “if current trends hold true, with microarchitectures continuing to become more complex and intricate as we achieve more breakthroughs in performance and scaling, we are moving full-speed toward a brick wall – power consumption.”

Nanotechnology may offer solutions to some of the issues with future scaling of CMOS technology. Most likely the computational “brains” of future SoC’s (Systems on a Chip) will be multiple CMOS cores and DSPs (as limited by the scaling roadblocks) augmented with nanotechnology “brawn.” Global on-chip metal wires may be replaced with strategically located strapped on nanotubes, I/O pads may be largely replaced with nanotech/MEMS sensors and actuators (chips that see, smell, hear, taste), low power nanotech alternatives for wireless communication components will emerge, and radically new high density, nonvolatile, on-chip storage technologies are already on the horizon. Additionally, the use of nanotechnology as these brawn parts may help to mitigate power consumption and to reduce mask costs (due to the use of technologies that self assemble). However, the issues of increasing design costs and error rates will be further exacerbated by the introduction of nanotechnology onto the SoC. New design aides that support the combination of heterogeneous technologies must be developed. Some of the fundamental issues that have long driven computer architecture research (e.g., the memory bottleneck may evaporate) will morph into issues focused on fault tolerance and low power.

Thus, my proposal for a “grand research challenge” in computer science and engineering is how to most effectively combine the best of future CMOS with the best of future nanotechnologies to produce cheap, high performance, low power, small form factor, mobile networked ubiquitous computers. Ubiquitous computing will emerge only when computation, sensing and communication are essentially free. This will require revolutionary progress in heterogeneous SoC design and design aides, radically different computer architectures, and innovative system software (compilers, run-time systems, wireless communications protocols, applications codes) that make the most effective use of these radically different computer architectures.

## **Biography**

Dr. Irwin received her Ph.D. degree in computer science from the University of Illinois in 1977. Her current research and teaching interests include computer architecture, embedded and mobile computing systems design, low power design, and electronic design automation. She was named a Fellow of The Institute of Electrical and Electronic Engineers (IEEE) in 1995 and a Fellow of The Association for Computing Machinery (ACM) in 1996. She received an Honorary Doctorate from Chalmers University, Sweden, in 1997 and the Penn State Engineering Society's Premier Research Award in 2001. Dr. Irwin is currently serving as chair of the National Science Foundation's Computer Information Sciences and Engineering Directorate's Advisory Committee, as a member of the Technical Advisory Board of the Army Research Lab, as the Editor-in-Chief of ACM's Transaction on Design Automation of Electronic Systems, and as an elected member of the Computing Research Association's Board of Directors. In the past she has served as an elected member of the IEEE Computer Society's Board of Governors, of ACM's Council, and as Vice President of ACM. She and her husband Vern celebrated their 35th wedding anniversary in July 2001 and (finally!) became grandparents on March 19, 2002.